Etch (ME) etch using fluorine chemistry is used to achieve vertical sidewalls, as is well known to those skilled in the art.

[0082] FIG. **66** shows the substrate in cross section following photoresist removal. An oxygen plasma is used to burn off any remaining photoresist.

[0083] FIG. **67** shows the substrate in cross section following the deposition of titanium nitride (TiN) **671**. A sputterer or Atomic Layer Deposition (ALD) is used to deposit a thin adhesion layer of TiN. This layer will help the subsequent tungsten layer to stick to the oxide.

[0084] FIG. **68** shows the substrate in cross section following the deposition of tungsten **681**. Tungsten is used because it has good conductivity and it deposits conformally (via CVD) and can fill the contact holes. The tungsten thickness must be at least half of the diameter of the contact hole.

[0085] FIG. **69** shows the substrate in cross section following the planarization of the tungsten. CMP is used to remove the surface tungsten. The surface titanium nitride is also removed as well. The remaining tungsten forms contact "plugs". These contact plugs are the contacts that are used to connect the transistor contacts and non-memory diode contacts to the metal interconnects that will be formed during the back end of line (BEOL) processing.

[0086] FIG. **70** shows the substrate in cross section following the spin-on, exposure, and development of the photoresist **701** to once again define the diode array areas for the formation of the information storage elements. This is the third and final use of this non-critical mask. Note that if diodes other than memory cell diodes are present in the array formation (i.e., diodes for which an information storage element is not desired), then a new mask will have to be created so as to mask away any diodes not having an information storage element.

[0087] FIG. **71** shows the substrate in cross section following a tungsten etch. An RIE etch will selectively remove the tungsten on top of the memory diodes, leaving the field oxide and forming cups **711** where information storage elements are to be formed.

[0088] FIG. **72** shows the substrate in cross section following photoresist removal. An oxygen plasma is used to burn off any remaining photoresist.

[0089] FIG. **73** shows the substrate in cross section following the deposition of a silicon nitride layer **731** using Chemical Vapor Deposition (CVD). This is the same as the first step of forming a nitride spacer as is well known in the art.

[0090] FIG. **74** shows the substrate in cross section following a timed nitride etch to form spacer sidewalls. This is a carefully controlled Reactive Ion Etch (RIE) etch that removes the thin nitride from the horizontal surfaces, but will leave the silicon nitride on the lower sidewalls of the cups. These sidewalls will narrow the diameter of the cup such that this narrowed region **741** will concentrate the current density in the information storage element material. This will result in lower power requirements when the cup is filled with a Chalcogenide material.

[0091] FIG. **75** shows the substrate in cross section following sputter deposition or MOCVD deposition of a phase-change material **751** such as a Chalcogenide alloy such as GST. (i.e., an alloy of elements including Germanium, Tellurium and Antimony). The Chalcogenide alloy thickness must be at least half of the diameter of the contact hole.

[0092] FIG. **76** shows the substrate in cross section following the planarization of the Chalcogenide alloy. CMP is used to remove the surface Chalcogenide alloy. The resulting surface will have contact points of tungsten (at the device contacts) and GST (at the information storage elements **0**.

[0093] Only the interconnect wiring of the metal layers remains to be done. This is done the same as is done in a standard CMOS process. FIG. **77** shows the substrate in cross section following two back end of line (BEOL) metal layers of interconnects. The present example figures also presumes that the source and drain contacts to the PMOS transistor and the gate contact to the NMOS transistor are formed in a plane other than that plane of the cross section of the figures and are therefore not depicted. The interconnect would be followed by the formation of the bond pads and passivation. All of this, as well as the specifics of the many individual process steps described above, are all well understood by those skilled in the art. However, a key aspect of the present invention is the ordering of the steps such that the transistors and the diodes are formed with salicided contacts while the phase-change material is not subjected to high (above 800.degree. C.) temperatures.

[0094] Devices constructed according to the present invention can be incorporated into memory card controller chips so as to combine the functions of the controller with the information storage circuitry in a single chip. Devices so constructed will find applicability in such areas as memory devices for storing digital text, digital books, digital music, digital audio, digital photography (wherein one or more digital still images can be stored including sequences of digital images), digital video, and digital cartography (wherein one or more digital maps can be stored), as well as any combinations thereof. These devices can be removable or removable and interchangeable among electronic systems that use memory cards. They can be packaged in any variety of industry standard form factors including Compact Flash, Secure Digital, MultiMedia Cards, PCMCIA Cards, Memory Stick, any of a large variety of integrated circuit packages including Ball Grid Arrays, Dual In-Line Packages (DTP's), SOIC's, PLCC, TQFP's and the like, as well as in custom designed packages. These packages can contain just the combined controller with memory chip, multiple memory chips, one or more memory chips along with other logic devices or other storage devices such as PLD's, PLA's, micro-controllers, microprocessors or chip-sets or other custom or standard circuitry.

[0095] The foregoing description of an example of the preferred embodiment of the invention and the variations thereon have been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by any claims appended hereto.

What is claimed is:

1. A CMOS device, comprising:

a doped silicon substrate;

a doped epi silicon layer formed over the doped silicon substrate;

a first p-doped well disposed within the doped epi silicon layer;

an n-doped bitline coupled to the first p-doped well;